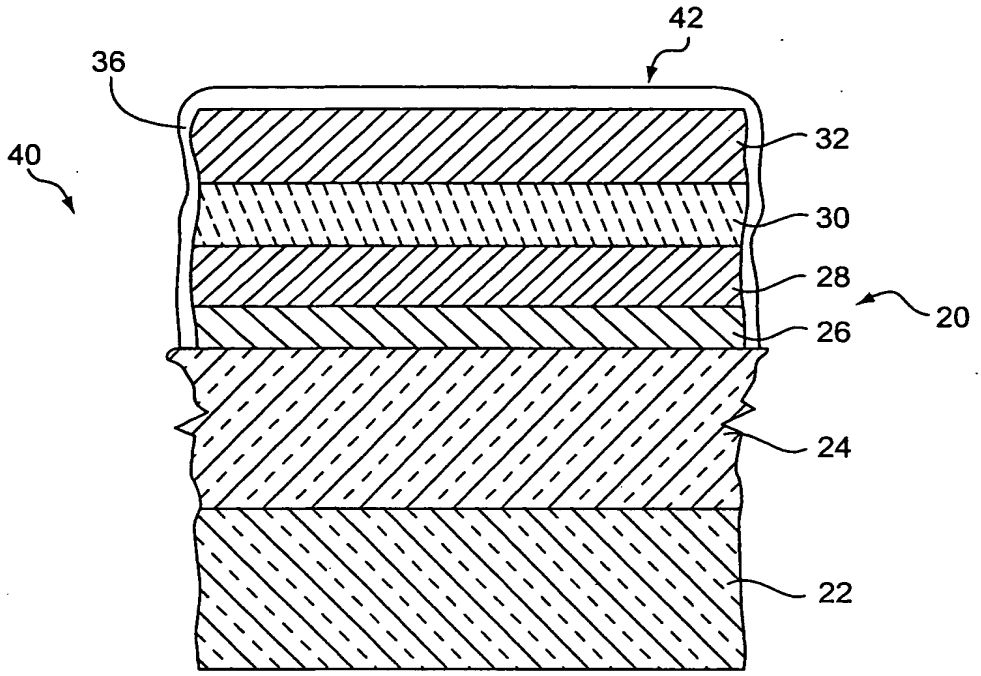
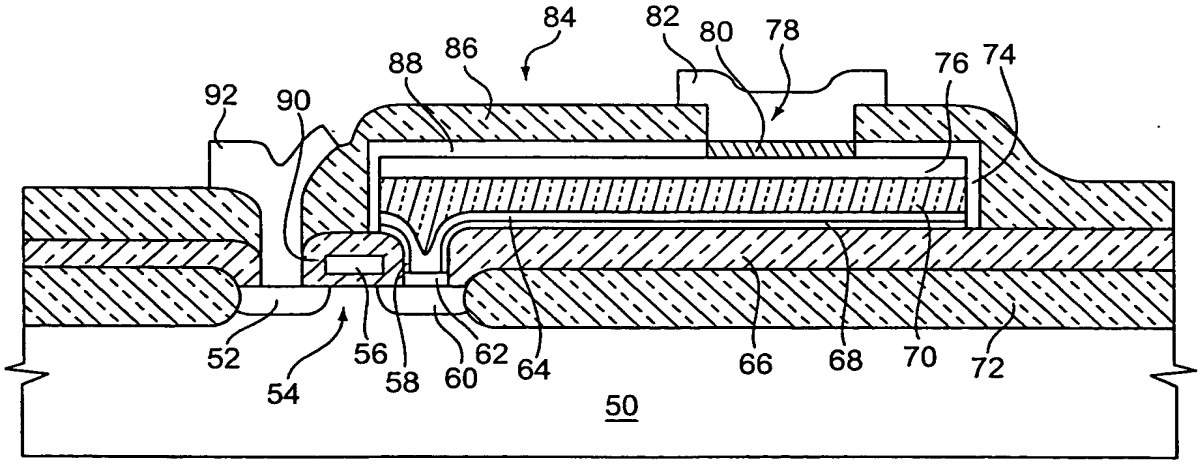

42
36
40
32
30
28
20
26
24
22

FIG. 1

FIG. 2


84
82
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88
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76
74
92
90
52
54
56
58
60
62
64
66
68
70
72
50

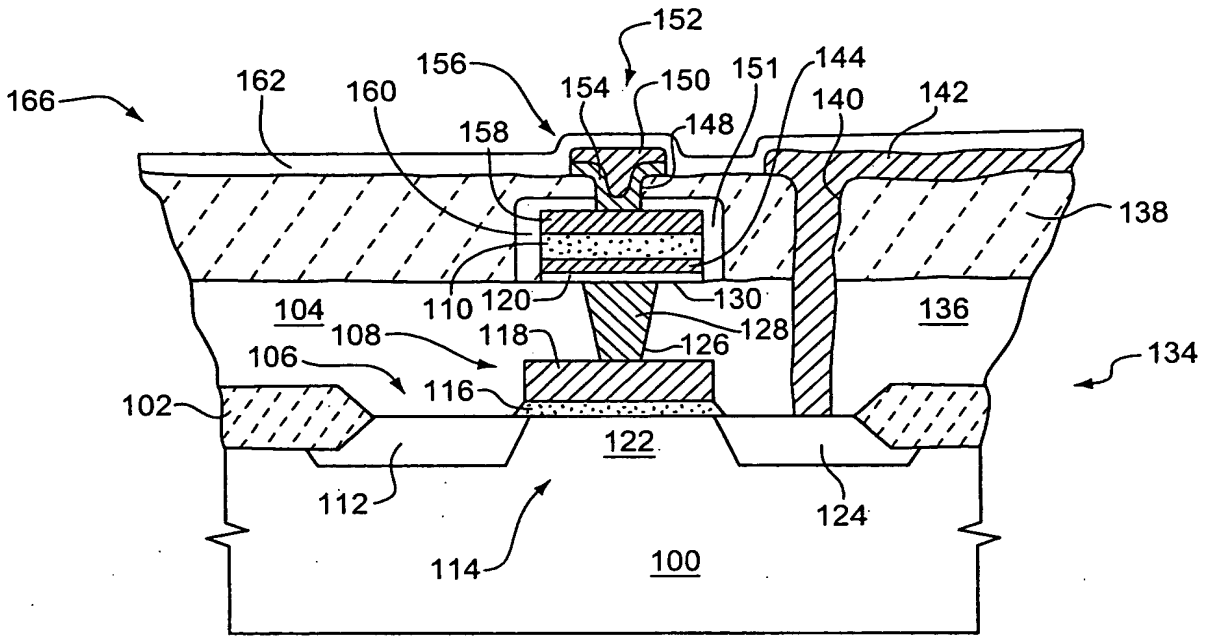
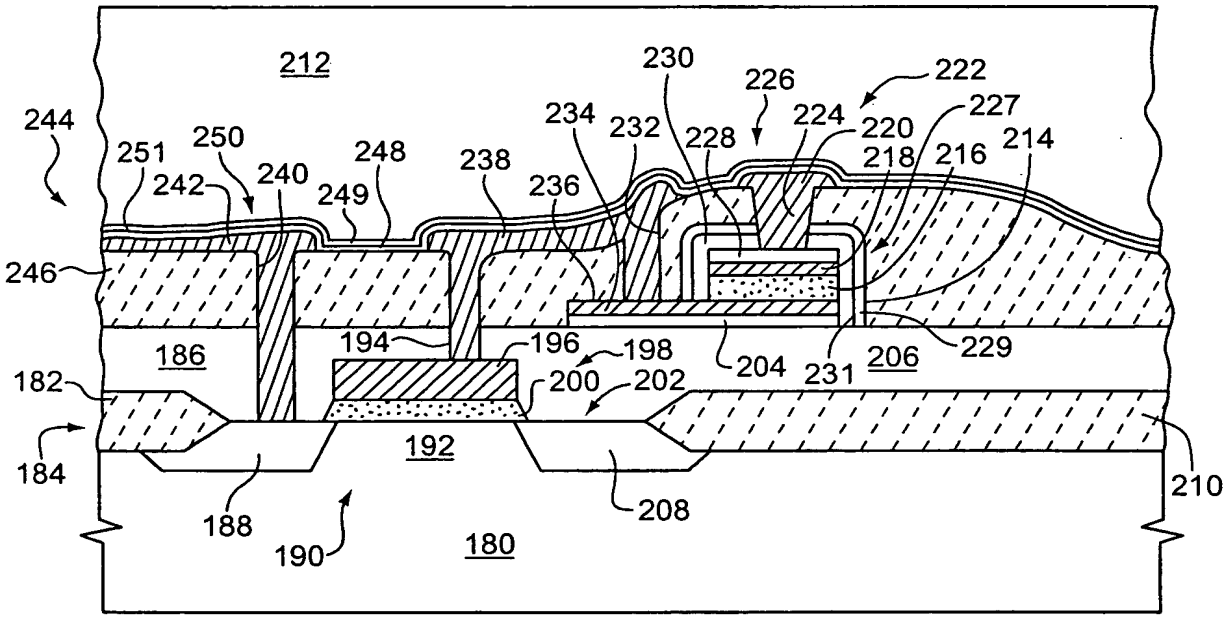

152
156
154
150
151
144
166
162
160
140
142
158
148
138
104
110
120
130
136
108
118
128
106
126
134
116
102
122
112
124
114
100

FIG. 3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230
226
222
244
234
232
228
224
227
251
250
220
214
242
240
248
238
236
218
216
246
249
194
196
198
204
231
206
229
186
182
200
202
192
184
210
188
208
190
180

FIG. 4

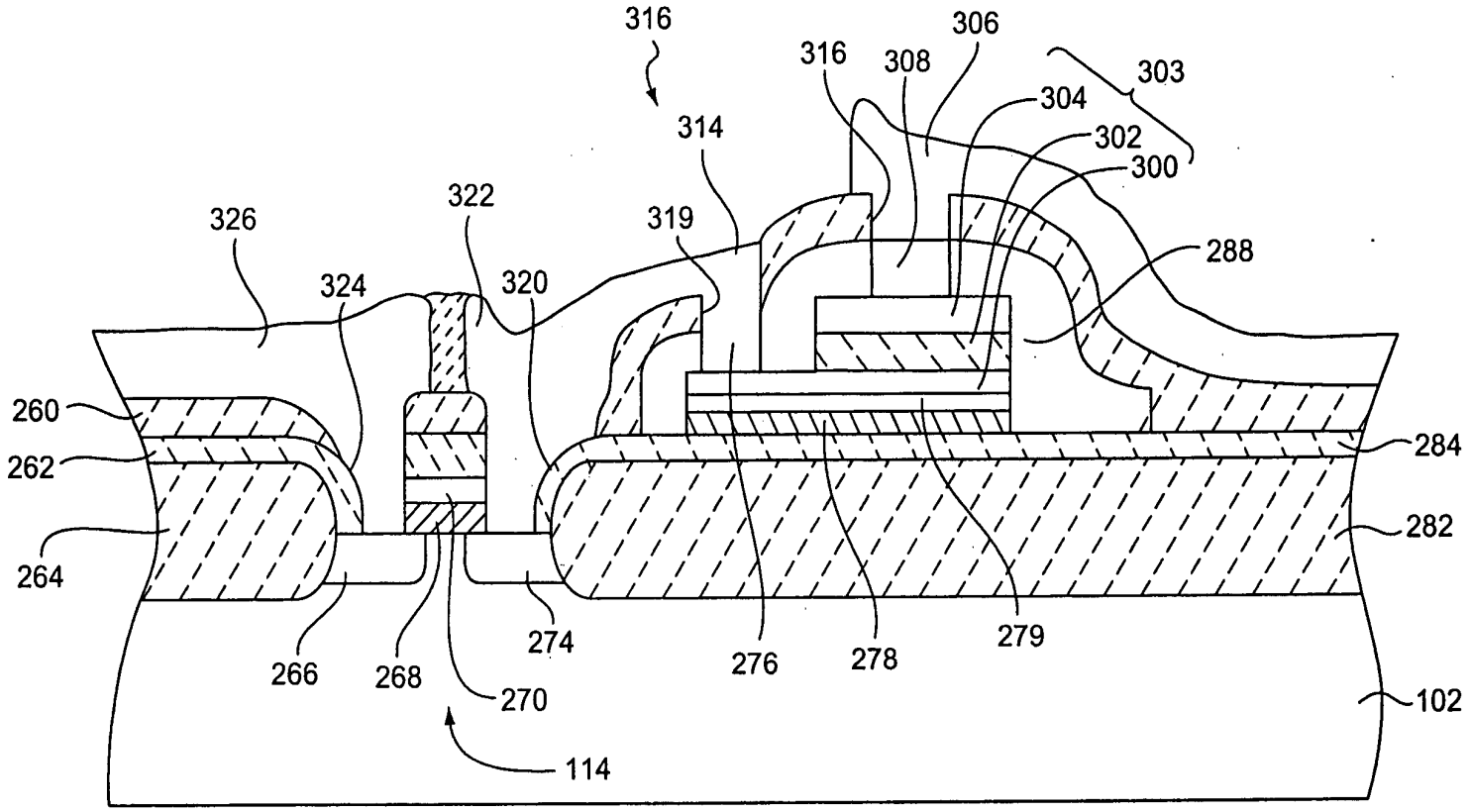

316
316
308
306
303
304
314
302
300
322
319
326
324
320
288
260
262
284
264
282
266
268
274
276
278
279
270
102
114

FIG. 5

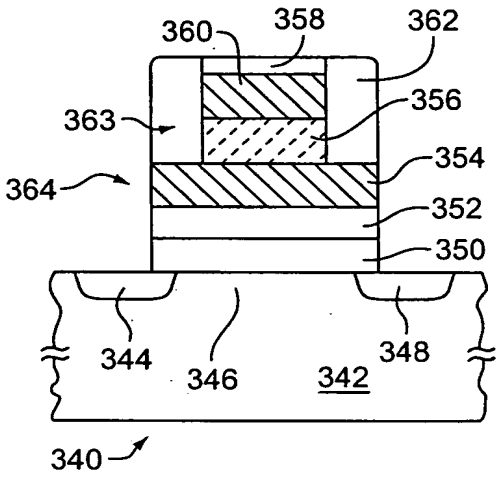

360
358
362
356
363
354
364
352
350
344
346
348
342
340

FIG. 6

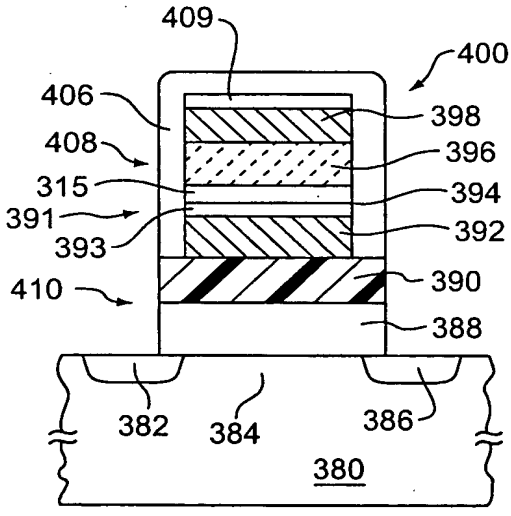

409
400
406
398
408
396
315
394
391
392
393
390
410
388
382
384
386
380

FIG. 7

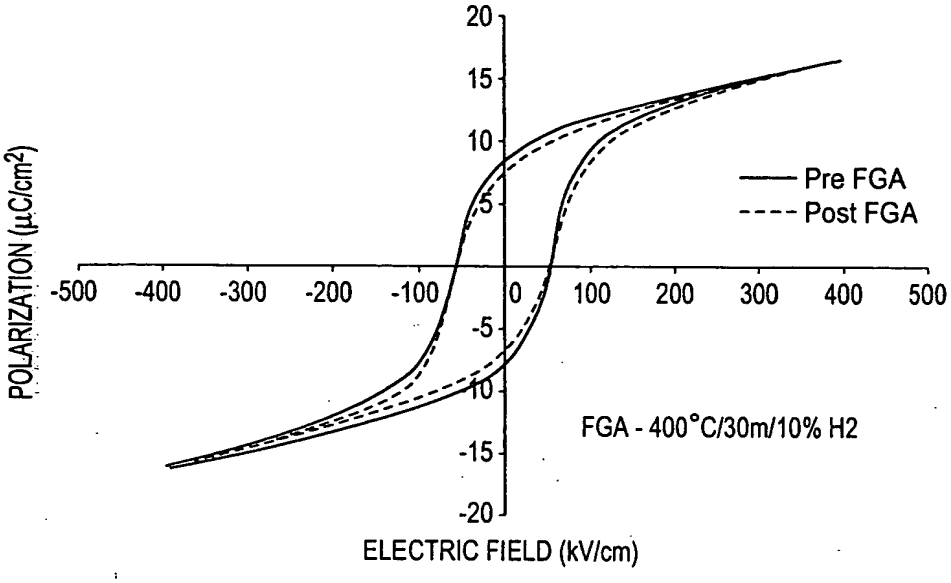

POLARIZATION (μC/cm²)
20
15
10
5
-5
-10
-15
-20
-500
-400
-300
-200
-100
0
100
200
300
400
500
Pre FGA
Post FGA
FGA - 400°C/30m/10% H2
ELECTRIC FIELD (kV/cm)

FIG. 8

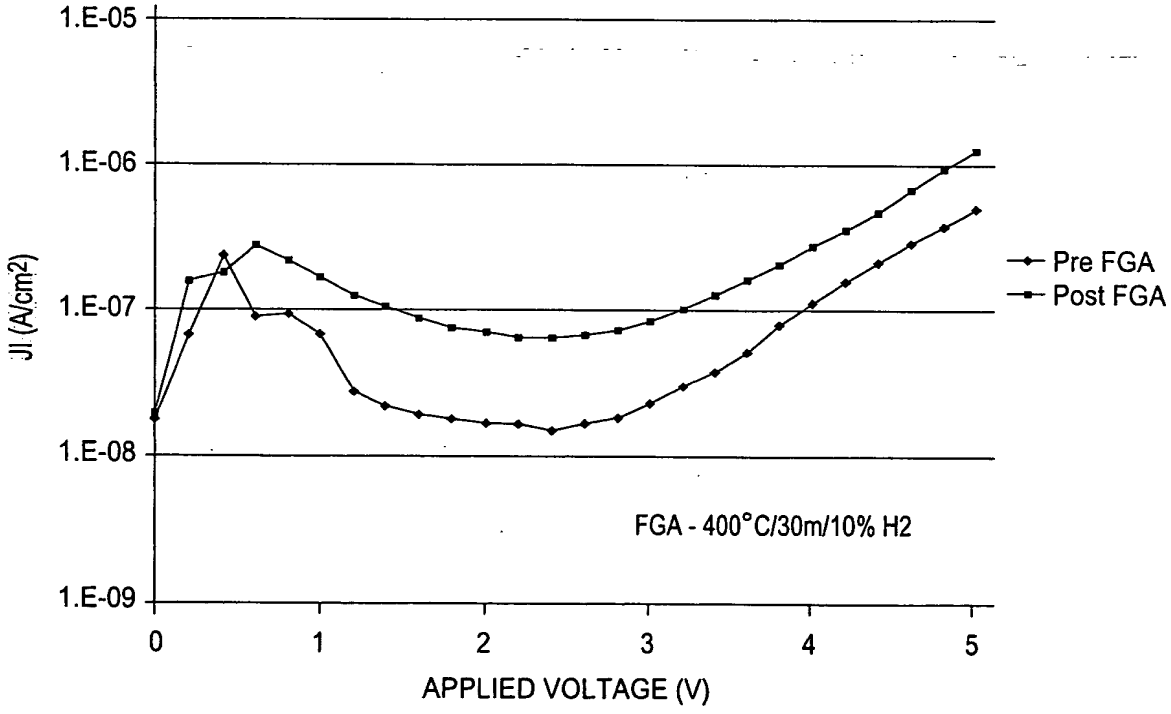

JI (A/cm²)
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
0
1
2
3
4
5
Pre FGA
Post FGA
FGA - 400°C/30m/10% H2
APPLIED VOLTAGE (V)

FIG. 9

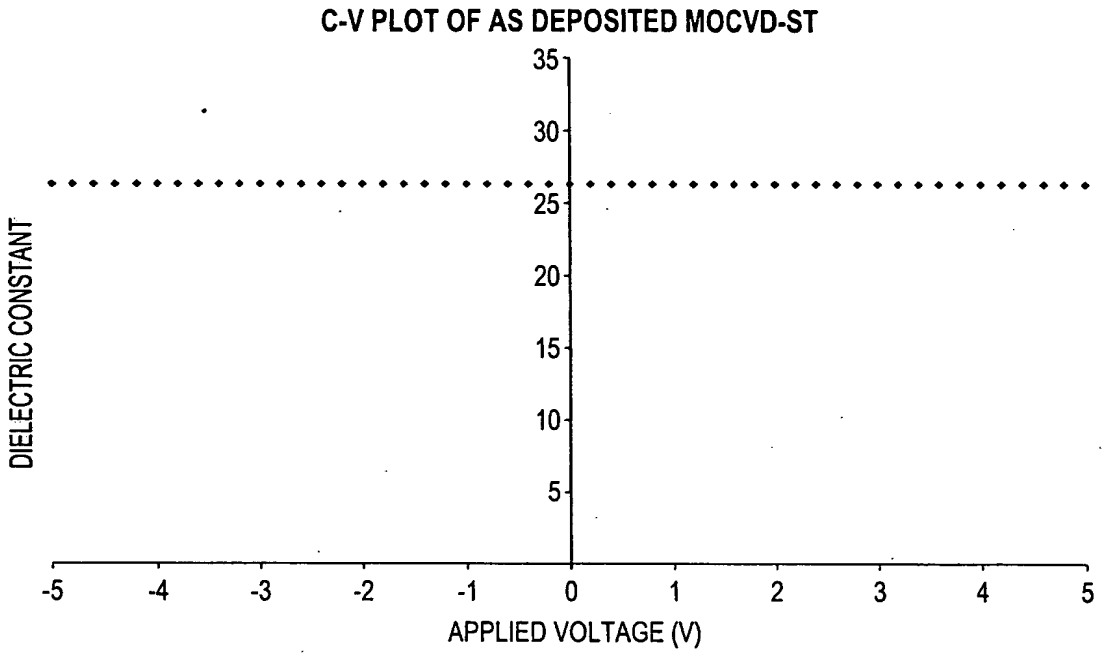

C-V PLOT OF AS DEPOSITED MOCVD-ST
DIELECTRIC CONSTANT
35
30
25
20
15
10
5
-5
-4
-3
-2
-1
0
1
2
3
4
5
APPLIED VOLTAGE (V)

FIG. 10

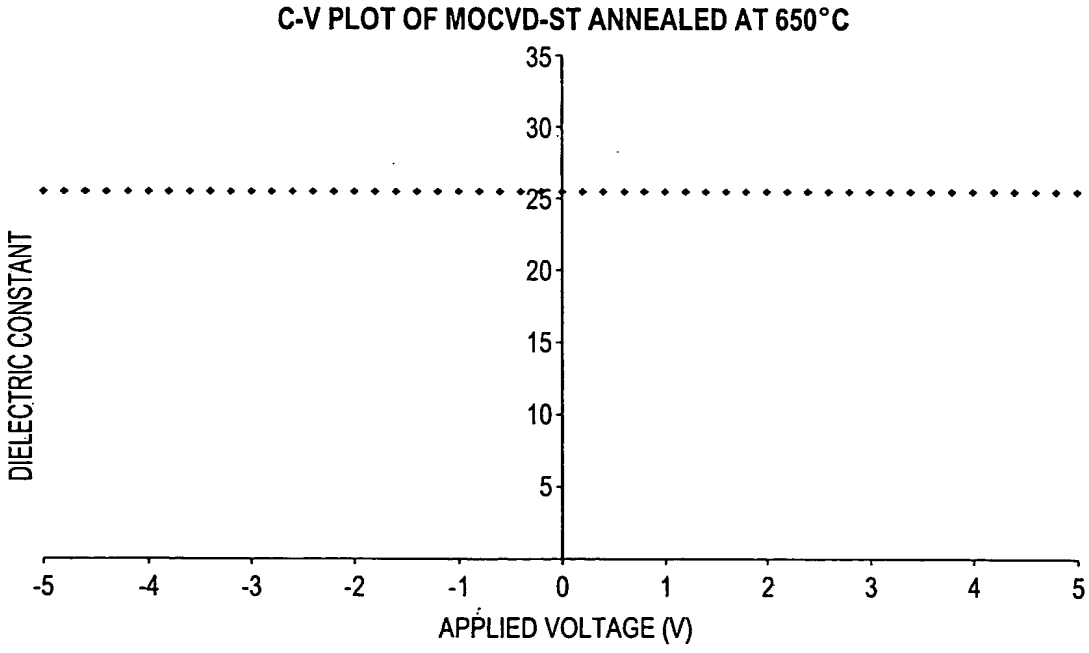

C-V PLOT OF MOCVD-ST ANNEALED AT 650°C
DIELECTRIC CONSTANT
35
30
25
20
15
10
5
-5
-4
-3
-2
-1
0
1
2
3
4
5
APPLIED VOLTAGE (V)

FIG. 11

FIG. 12

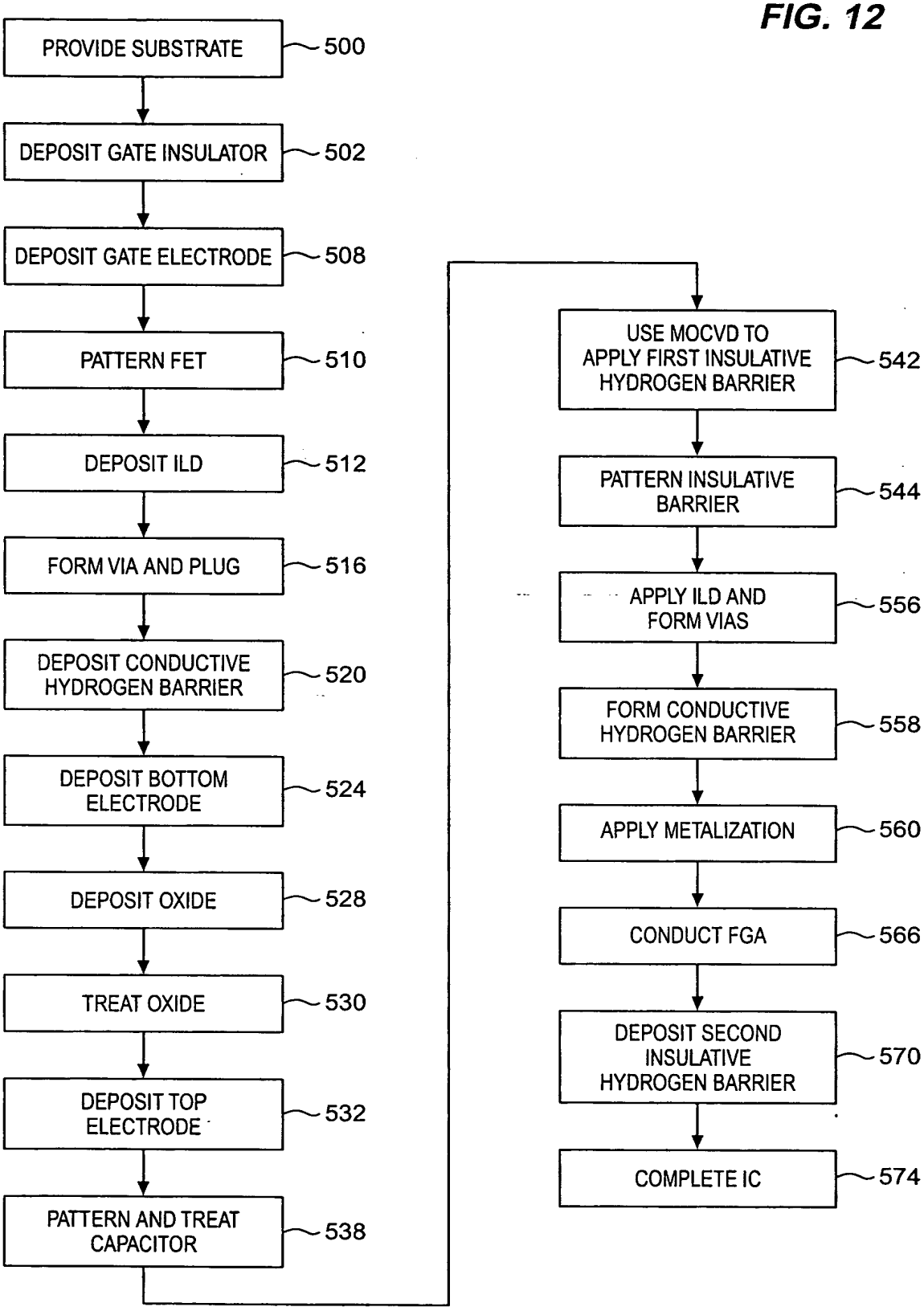

PROVIDE SUBSTRATE
500
DEPOSIT GATE INSULATOR
502
DEPOSIT GATE ELECTRODE
508
PATTERN FET
510
DEPOSIT ILD
512
FORM VIA AND PLUG
516
DEPOSIT CONDUCTIVE HYDROGEN BARRIER
520
DEPOSIT BOTTOM ELECTRODE
524
DEPOSIT OXIDE
528
TREAT OXIDE
530
DEPOSIT TOP ELECTRODE
532
PATTERN AND TREAT CAPACITOR
538
USE MOCVD TO APPLY FIRST INSULATIVE HYDROGEN BARRIER
542
PATTERN INSULATIVE BARRIER
544
APPLY ILD AND FORM VIAS
556
FORM CONDUCTIVE HYDROGEN BARRIER
558
APPLY METALIZATION
560
CONDUCT FGA
566
DEPOSIT SECOND INSULATIVE HYDROGEN BARRIER
570
COMPLETE IC
574

FIG. 13

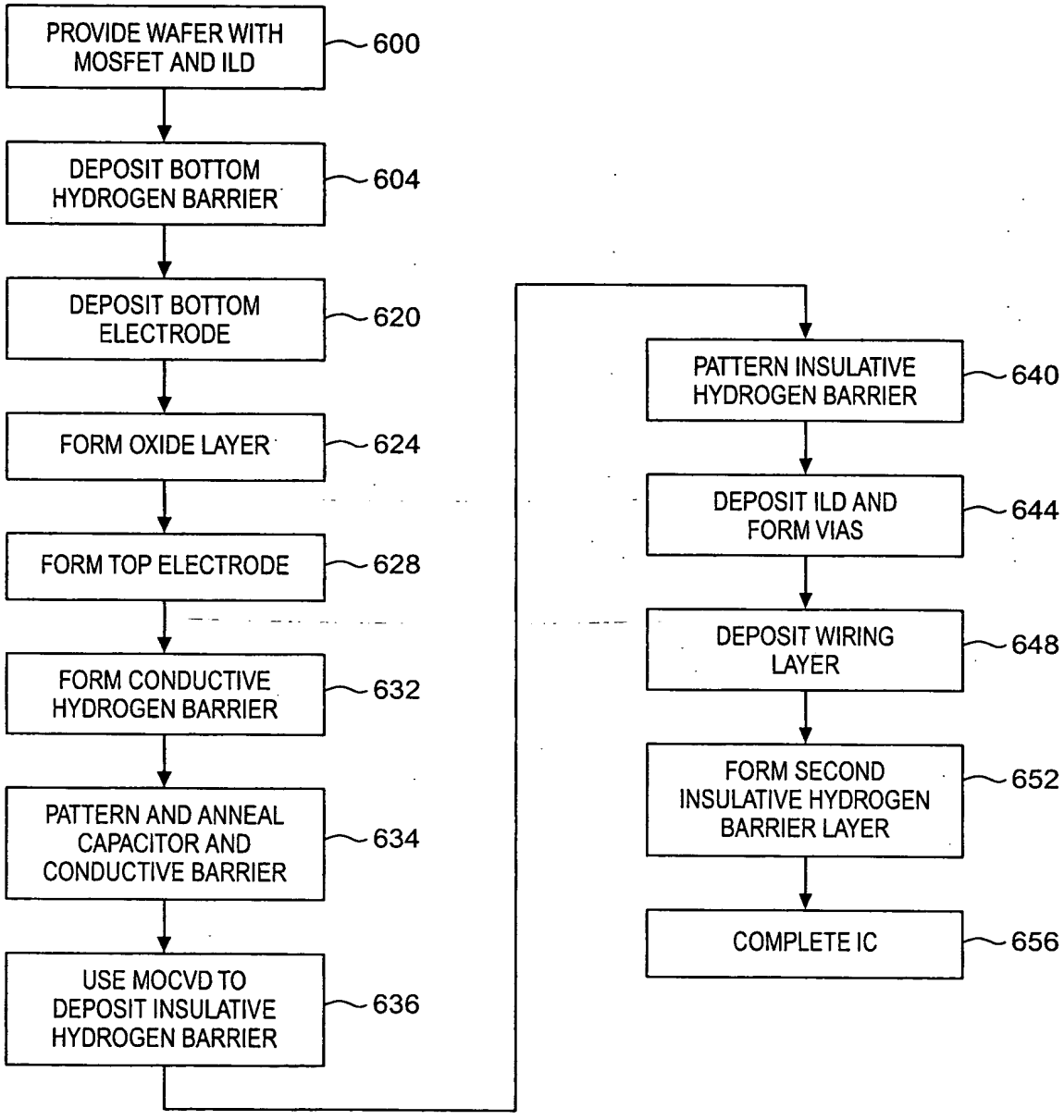
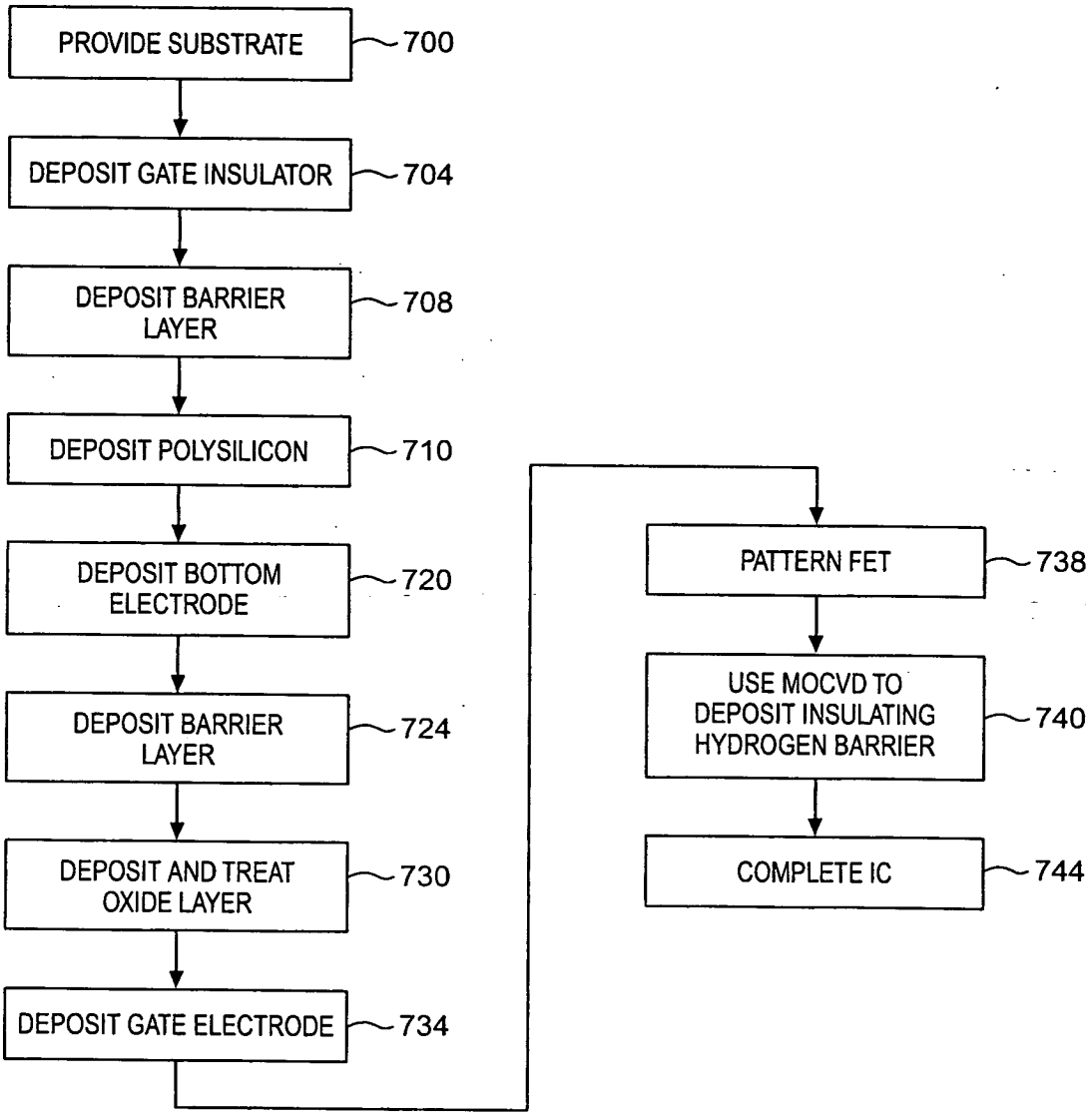

PROVIDE WAFER WITH MOSFET AND ILD
600
DEPOSIT BOTTOM HYDROGEN BARRIER
604
DEPOSIT BOTTOM ELECTRODE
620
FORM OXIDE LAYER
624
FORM TOP ELECTRODE
628
FORM CONDUCTIVE HYDROGEN BARRIER
632
PATTERN AND ANNEAL CAPACITOR AND CONDUCTIVE BARRIER
634
USE MOCVD TO DEPOSIT INSULATIVE HYDROGEN BARRIER
636
PATTERN INSULATIVE HYDROGEN BARRIER
640
DEPOSIT ILD AND FORM VIAS
644
DEPOSIT WIRING LAYER
648
FORM SECOND INSULATIVE HYDROGEN BARRIER LAYER
652
COMPLETE IC
656

FIG. 14


PROVIDE SUBSTRATE
700
DEPOSIT GATE INSULATOR
704
DEPOSIT BARRIER LAYER
708
DEPOSIT POLYSILICON
710
DEPOSIT BOTTOM ELECTRODE
720
DEPOSIT BARRIER LAYER
724
DEPOSIT AND TREAT OXIDE LAYER
730
DEPOSIT GATE ELECTRODE
734
PATTERN FET
738
USE MOCVD TO DEPOSIT INSULATING HYDROGEN BARRIER
740
COMPLETE IC
744